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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/065,212	09/26/2002	Raj Kumar Jain	2000P19188US	8176

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EXAMINER	
LE, THONG QUOC	
ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 11/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/065,212	JAIN, RAJ KUMAR	
	Examiner	Art Unit	
	Thong Q. Le	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-19 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-4,13-15,17 and 18 is/are rejected.

7)☒ Claim(s) 5-12,16 and 19 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. Claims 1-19 are presented for examination.

Specification

2. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Drawings

3. The drawings in this application are objected to by the Draftsperson as informal. Any drawing corrections requested, but not made in the prior application should be repeated in this application if such changes are still desired. If the drawings were changed and approved during the prosecution of the prior application, a petition may be filed under 37 CFR 1.182 requesting the transfer of such drawings, provided the parent application has been abandoned. However, a copy of the drawings as originally filed must be included in the 37 CFR 1.60 application papers to indicate the original content.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-4, 13-15, 17-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Taylor (U.S. Patent No. 5,844,856).

Regarding claim 1, 13-14, 17 Taylor discloses an IC (Figure 1) comprising :

a memory cell array having a plurality of memory cells (Figure 2);

a first ((Figure 2, 118) and a second port (Figure 2, 120) , each of memory cells being coupled to the first and second ports (Figure 2) ;

a cache memory (Figure 5, 500, Column 1, lines 51-67, Column 2, lines 1-10) coupled to the first and second ports (Column 1, lines 50-65), wherein during a read operation subject to one of the memory cell through one of the first and second ports a data stored in one of the memory cells is read out from the cache memory if it is determined that the cache memory contains the data stored in one of the memory cells (Column 1, lines 59-65, Column 9, lines 33-37); and a refresh control circuit (Column 7, lines 8-10) performing a refresh of the information stored within the memory cells , the refresh control circuit refreshing memory cell through on of the ports while reading data out of the cache memory (Column 5, lines 45-48, Column 7, lines 35-65). More specifically, Taylor discloses memory cell array having a plurality of dynamic memory cell (Column 4, lines 44) as claim 13 discloses.

Regarding claims 2, 15, Taylor discloses the cache memory comprises a tag portion and address portion, and a data portion corresponding to each other, and the tag portion indicates if the corresponding address and data portions contain a valid address and data value (Column 51-65, Column 9, lines 33-38).

Regarding claims 3-4, Taylor discloses the first and second ports each comprising an address path and a data read path, the address paths of the first and second ports being connected to the address portion of the cache memory and the data

read paths of the first and second ports being connected to the data portion (Column 1, lines 51-65, Column 5, lines 30-67, Column 6, lines 1-61).

Regarding claim 18, Taylor discloses the refresh operation is performed for a row of memory cells through the second port, and a read command received through the cache memory in parallel to the refresh operation (Figure 1, Column 5, lines 30-52).

Allowable Subject Matter

6. Claims 5-12, 16, 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 5-12, 16, 19 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Taylor (U.S. Patent No. 5,844,856), and others, does not teach the claimed invention having address comparator Figure 1, 44 is designed to compare an address being provided through the at least one of the ports and an address being provided from the address portion of the address memory, and in case of a match designed to output the data stored in the corresponding memory cell onto the read path of the at least one port Figure 1, 20, 30 as claims 5-10 disclose, and each memory cell of memory cell array comprises a first selection transistor Figure 3, 112 coupled to the first port and a second selection transistor Figure 3, 115 coupled to the second port and a storage node Figure 3,111 connected to the first and second selection transistors as claims 11-12, 16, 19 disclose.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 703-306-9123. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on 703-308-4910. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-3329.

Thong Q. Le
Examiner
Art Unit 2818

October 29, 2004

THONG LE
PRIMARY EXAMINER